AMENDMENTS TO THE SPECIFICATION

Please replace paragraph starting on page 18, line 33 with the following amended paragraph:

The execution begins when the block diagram ~~440~~40 is compiled ~~442~~42. Following the compilation stage, is the model link stage ~~444~~44 which may also produce linear models ~~446~~46. Code may or may not be generated ~~445~~45. If code is generated ~~448~~48, a decision is made ~~449~~ 49 whether to continue the simulation. If the decision is made to continue the simulation the model is simulated/executed through the Simulation Loop ~~450~~50. If the simulation is not continued, the code may be delivered to a target ~~452~~52 and executed in an external mode ~~454~~54. If code is not generated the block diagram may execute in interpretive mode when entering the Simulation Loop ~~450~~50.

Please replace paragraph starting on page 20, line 10 with the following amended paragraph:

Once actual block connectivity has been determined (by removing the virtual blocks) the block diagram may be further optimized by performing block reduction and insertion. During this step, non-virtual blocks may be inserted or a set of non-virtual blocks may be completely removed or reduced to a single equivalent block. Block insertion and reduction is mainly done to improve execution efficiency. Examples of block insertion and reduction include the removal of Gain blocks whose gain value is 1. A Gain block is a block which multiplies its input value by a gain parameter, such as a simple amplifier. Figure 5 depicts the replacement of a collection of blocks ~~460~~60, ~~462~~62, and ~~464~~64 connected in an accumulator pattern and leading to result 66 with an equivalent synthesized block ~~468~~68 representing the accumulator pattern leading to the same result ~~466~~66. A signal copy block may also be automatically inserted in order to make contiguous memory copies of signals that are made up of disjoint memory sections. Block insertion and reduction may also be performed at other suitable stages of compilation.

Please replace paragraph starting on page 21, line 5 with the following amended paragraph:

The process of converting a block diagram into a compiled directed graph is shown in Figure 6A. A block diagram ~~481~~81 includes a Sine Wave 1 block ~~482~~82, a Sine Wave 2 block ~~484~~84, a Goto block ~~486~~86, a Function Call Generator block ~~488~~88, and a From block ~~490~~90. Also included are a Function Call Subsystem block ~~492~~92, a Sum block ~~494~~94, a Gain block ~~496~~96, an Integrator block ~~498~~98 and an Outport (Output 1) block 100. Those blocks which are not virtual or reduced appear on the corresponding directed graph 111. The directed graph 111 includes a Sine Wavel vertice 112, a Sine Wave 2 vertice 114, a function-call generator vertice 116, and a function call subsystem vertice 118. Also included are a Sum vertice 120, a Gain vertice 122, an Integrator vertice 124 and an Outport 1 vertice 126. The vertices are connected by arcs.

Please replace paragraph starting on page 30, line 31 with the following amended paragraph:

Figure 13 shows the overall sequence of steps taken by Simulink in multitask mode. Following initialization (step 220), the output method execution list is executed for the fastest sample time (step 222). The update method execution list is then executed for the fastest sample time (step 224). A time parameter is checked (step 225) to determine to determine if the time is less than a designated stop time. If the stop time has been reached, the simulation completes (step 226). Otherwise, the integrate stage (step 228) is performed. The task ID variable is incremented (step 230) and compared to a parameter of the number of sample times (step 231). If the task ID is less than the number of sample times, the output method execution list for the methods assigned the new task Id are executed (232) followed by the execution of the update method execution list assigned the new task ID (step 234). The task ID variable is incremented (step 236) and the process iterates with the task ID being compared to the number of sample rate times (step 231). When the task ID number is determined to equal the number of sample rate times, the simulation time is incremented (step 238) and the entire process iterates with the output method list execution list (step 222) being executed for the fastest sample times. The process continues until the end of simulation when the time equals the stop time (Step 226).
~~(Step 226).~~

Please replace the paragraph starting on page 40, line 1 with the following amended paragraph:

Figure 15 illustrates an environment suitable for practicing the illustrative embodiment of the present invention. A computer system 410 includes an electronic device 412, a network 424, such as the Internet, an intranet, or other suitable network either wired, wireless, or a hybrid of wired and wireless, and, optionally, a server 426 or other electronic device. The electronic device 412 includes a processor 418 for executing various instructions and programs, and controlling various hardware and software components. The electronic device 412 also includes a display device 420 for use in rendering textual and graphical images, a storage device 414 for storing various items such as data, information and programs. A keyboard 422 and a pointing device 424 are also included with the electronic device 412. The pointing device ~~426~~ 428 includes such devices as a mouse, track ball, or light pen. Those skilled in the art will recognize that the pointing device ~~426~~ 428 can be incorporated with the display device 420 to provide the electronic device 412 with a touch screen that allows a user to interact with the electronic device 412 with a stylus or other means such as a user's finger.

Please replace the paragraph starting on page 40, line 32 with the following amended paragraph:

The server 426 coupled to the network 424 includes the block diagram environment ~~16'~~416'. In this manner, a number of users are able to access the block diagram environment ~~16'~~ 416' via the network 424 without the need to have each user running a local copy of the block diagram environment 416. Those skilled in the art will recognize that the electronic device 412 includes other software such as, user interfaces and other programs, such as one or more OS programs, compilers and various other program applications developed in a variety of programming environments for controlling system software and hardware components.

Please replace the paragraph starting on page 42, line 3 with the following amended paragraph:

Figure 16 illustrates a block diagram model 430 suitable for use in practicing the illustrative embodiment of the present invention. The block diagram model 430 includes a first sub-system 432 coupled to a first gain block 436. The first gain block ~~36~~ 436 is coupled to a second sub-system 434, which, in turn, is coupled to an integration block ~~38~~438. The integration block 438 is also coupled to the first sub-system 432.

Please replace the paragraph starting on page 42, line 8 with the following amended paragraph:

The first sub-system 432 includes a first block 440 and a fourth gain block 442. The first block 440 receives an output from the integration block 432 and is capable of performing an operation on the output received from the integration block 438 or is alternately capable of passing the received output from the integration block 438 to an input of the fourth gain block 442. The fourth gain block 442 performs an operation to increase an amplitude of the signal received on the input. The first sub-system ~~32~~ 432 is a multi-rate system for the block 440 operates at a second operating rate, for example, 10 Hz and the fourth gain block 442 operates at a first operating rate, for example, 5 Hz.